Fig. 1

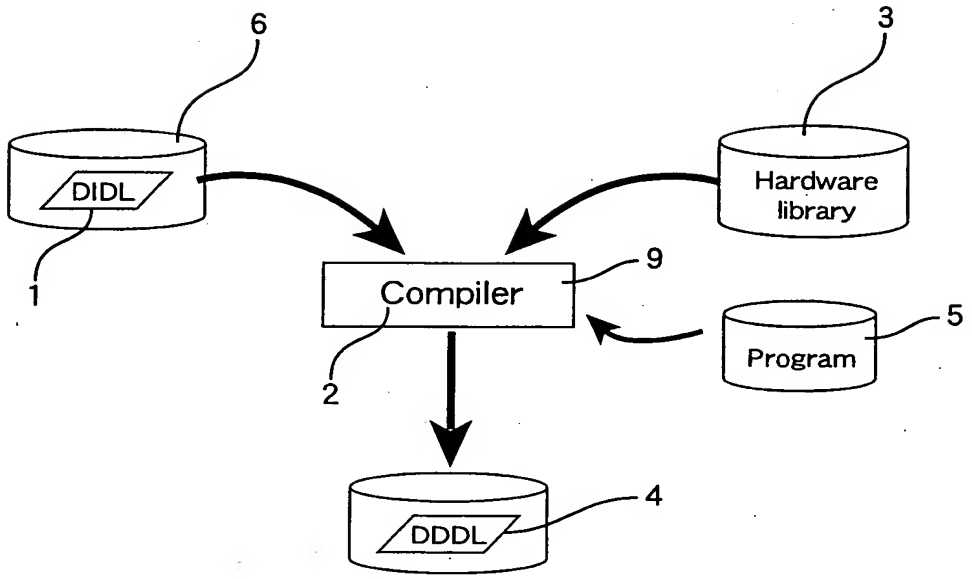


Fig. 2

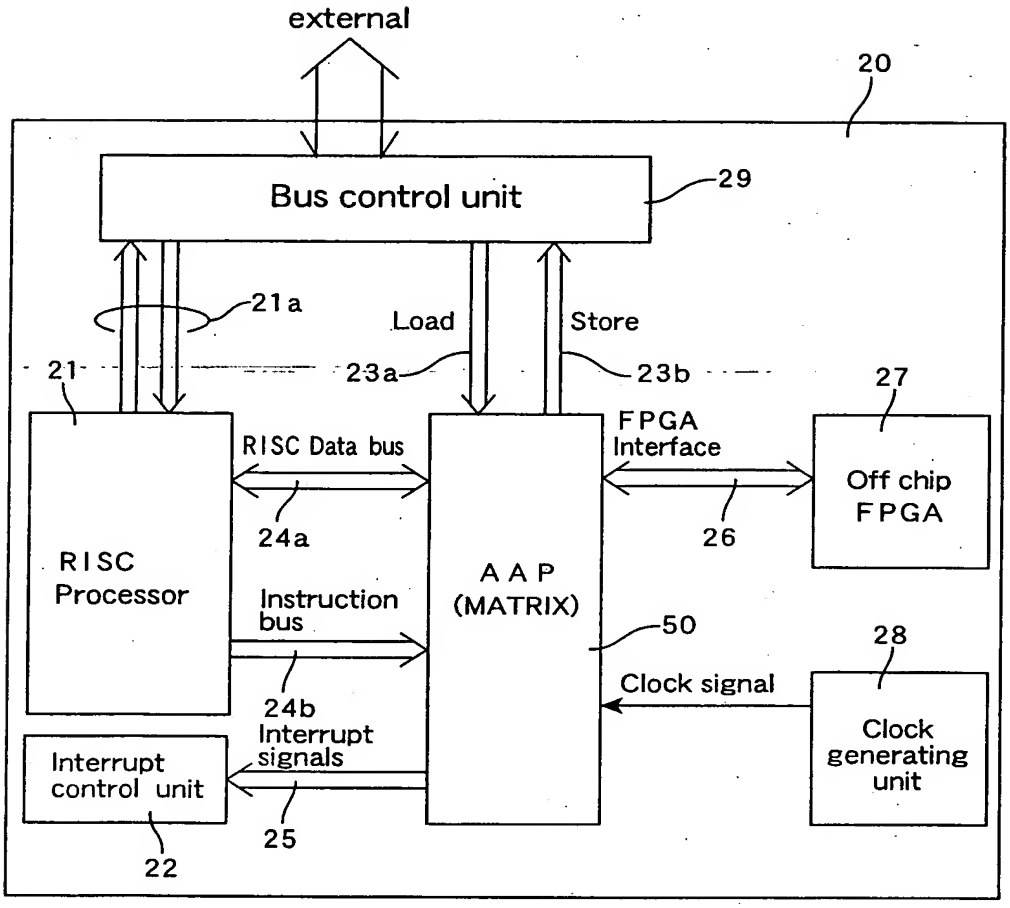

external
20
Bus control unit
29
21a
Load
Store
21
23a
23b
27
RISC Data bus
FPGA Interface
Off chip FPGA
24a
26
RISC Processor
Instruction bus
AAP (MATRIX)
50
28
Clock signal
24b
Interrupt signals
Clock generating unit
Interrupt control unit
25
22

Fig. 3

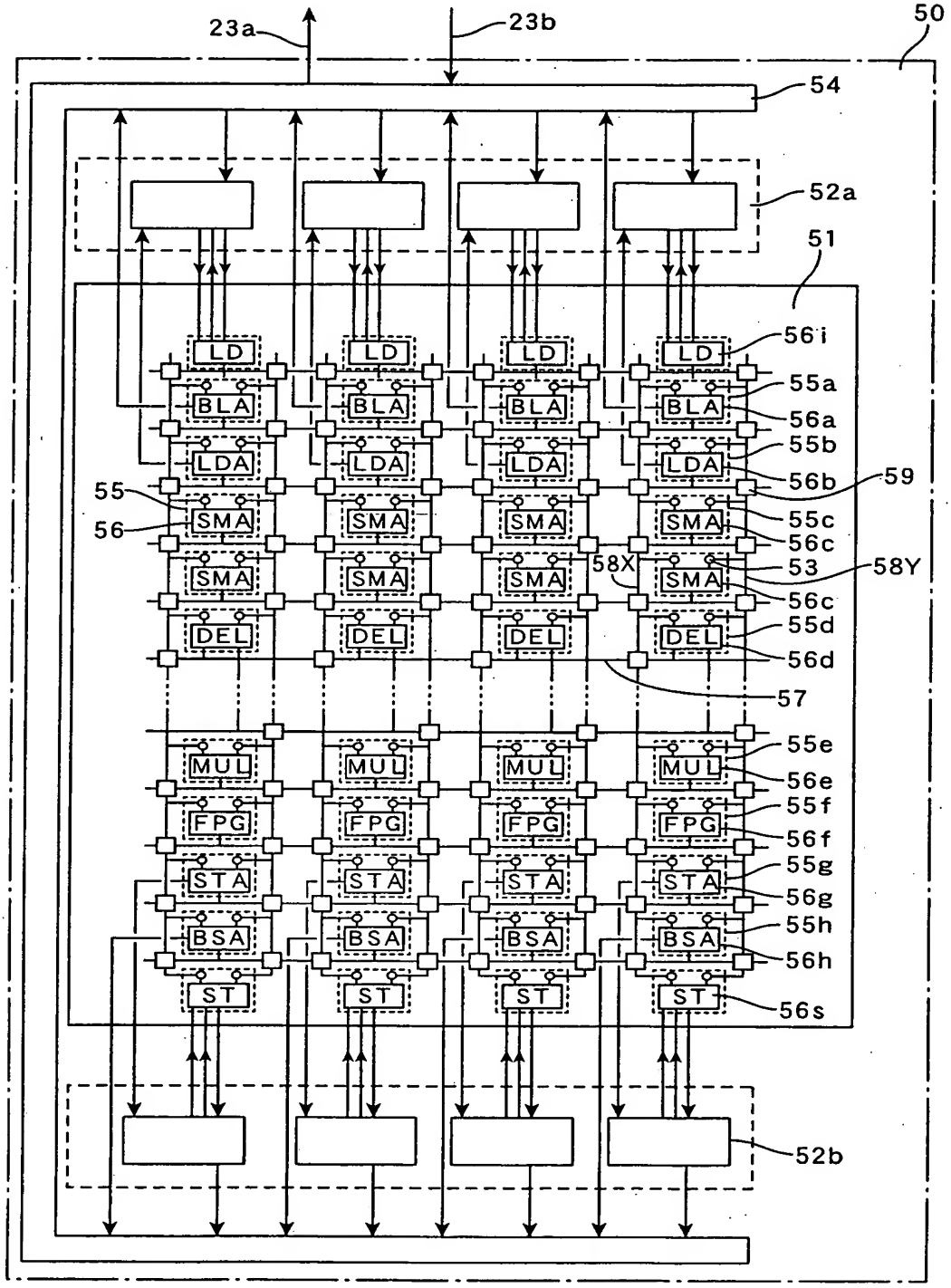

23a
23b
50
54
52a
51
56i
55a
56a
55b
56b
59
55
56
55c
56c
58X
53
58Y
56c
55d
56d
57
55e
56e
55f
56f
55g
56g
55h
56h
56s
52b
LD
BLA
LDA
SMA
DEL
MUL
FPG
STA
BSA
ST

Fig. 4

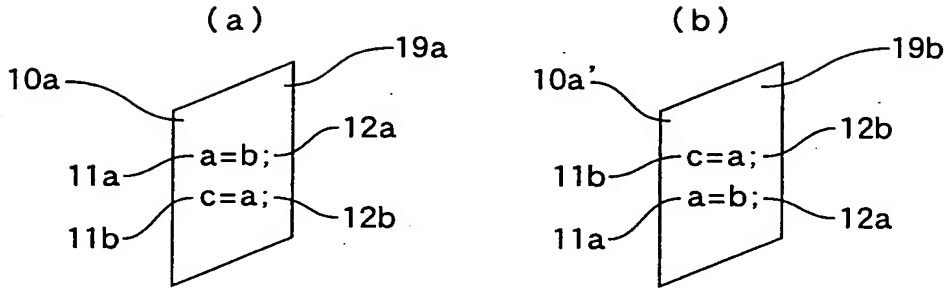

(a)
10a
19a
12a
a=b;
11a
c=a;
12b
11b
(b)
10a'
19b
12b
c=a;
11b
a=b;
12a
11a

Fig. 5

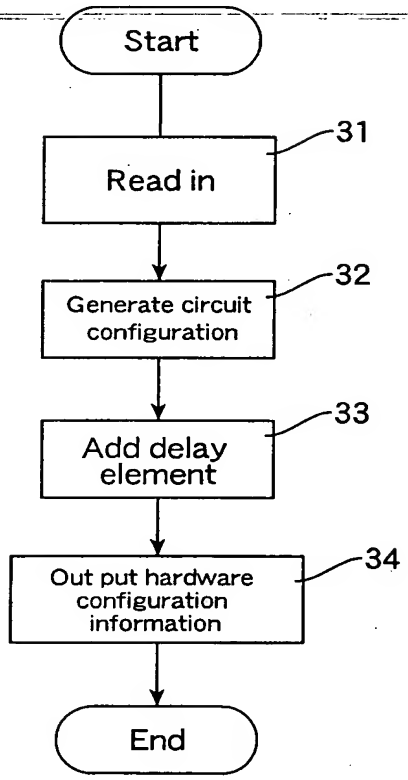

Start
31
Read in
32
Generate circuit configuration
33
Add delay element
34
Out put hardware configuration information
End

Fig. 6

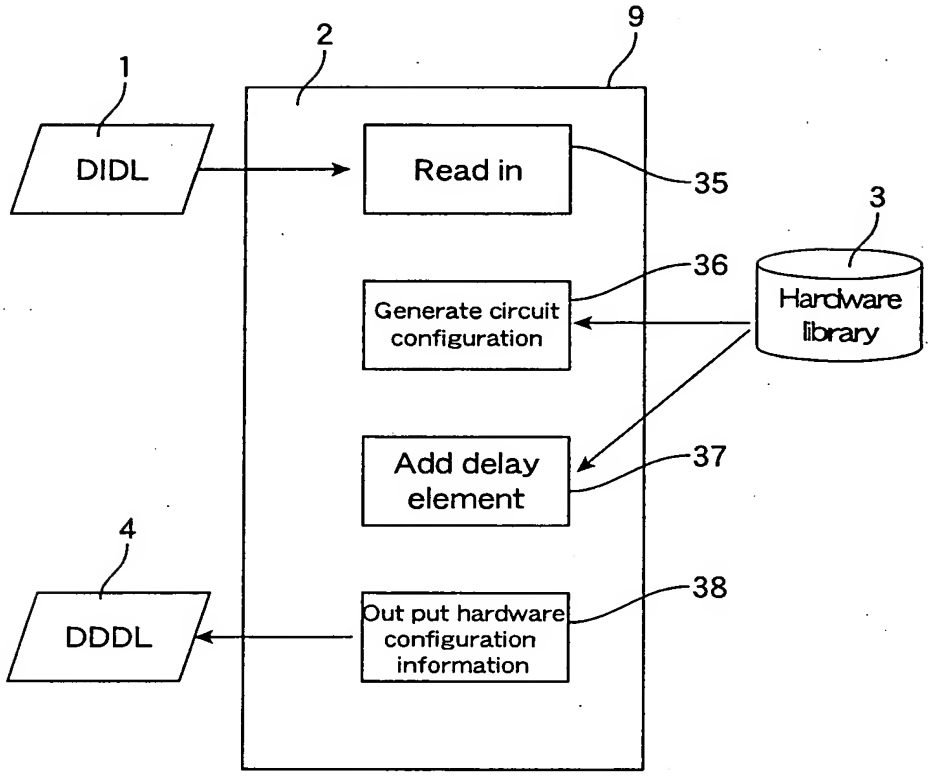

1
2
9
DIDL
Read in
35
3
36
Generate circuit configuration
Hardware library
Add delay element
37
4
DDDL
Out put hardware configuration information
38

Fig. 7

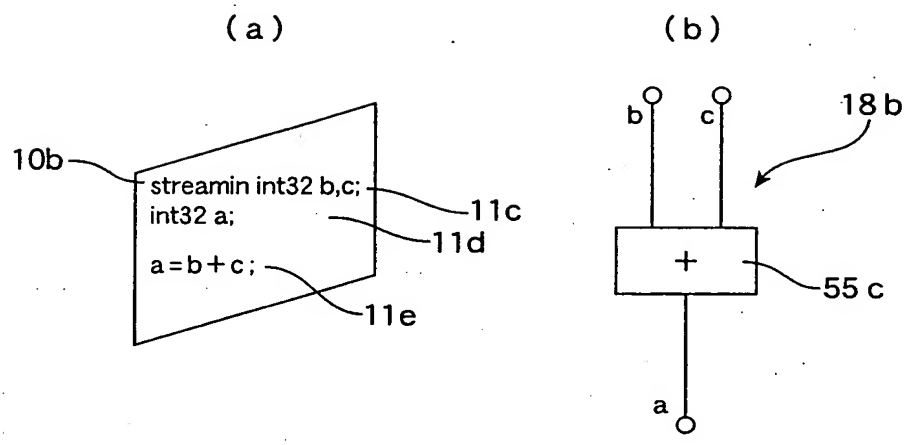

(a)
(b)
10b
streamin int32 b,c;
int32 a;
a=b+c;
11c
11d
11e
b
c
18b
+
55c
a

Fig. 8

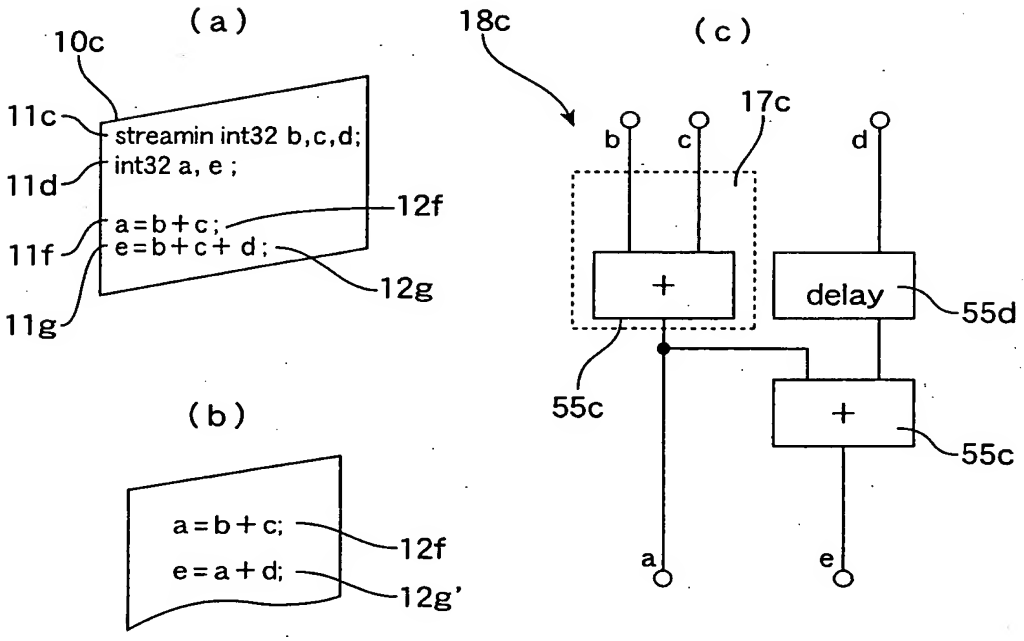

(a)
10c
11c
11d
11f
11g
streamin int32 b,c,d;
int32 a, e ;
a=b+c;
e=b+c+d;
12f
12g
(b)
a=b+c;
e=a+d;
12f
12g'
18c
(c)
17c
b
c
d
+
delay
55d
55c
+
55c
a
e

Fig. 9

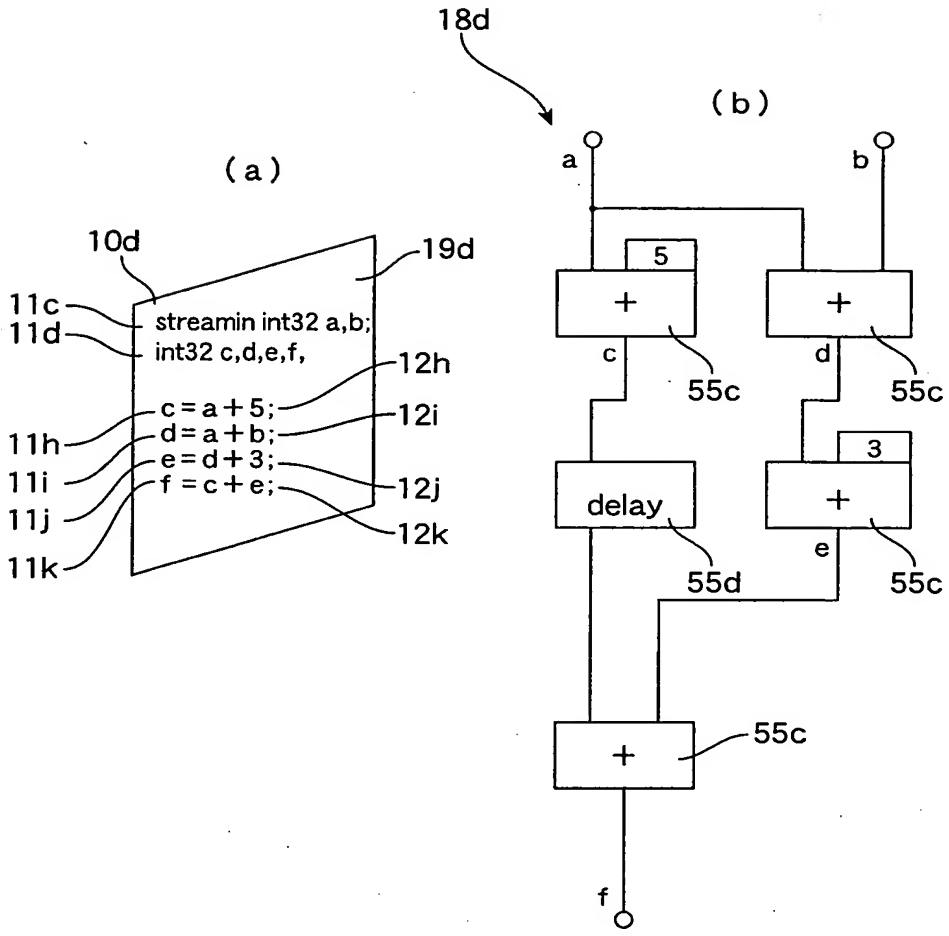

18d
(a)
(b)
10d
19d
11c
11d
streamin int32 a,b;
int32 c,d,e,f,
c = a + 5;
d = a + b;
e = d + 3;
f = c + e;
11h
11i
11j
11k
12h
12i
12j
12k
a
b
5
+
c
55c
d
55c
3
delay
55d
e
55c
55c
f

Fig. 10

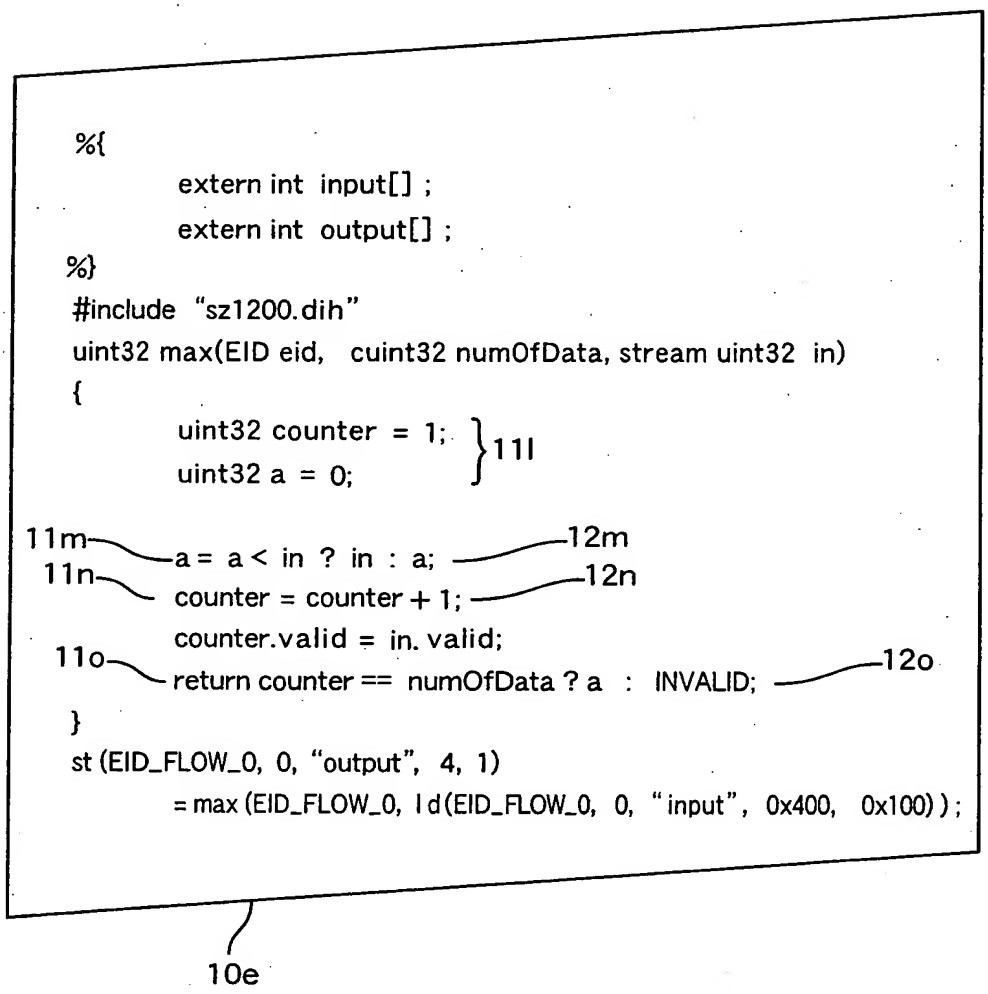

%{
extern int input[] ;
extern int output[] ;
%}
#include "sz1200.dih"
uint32 max(EID eid, cuint32 numOfData, stream uint32 in)
{
uint32 counter = 1;
uint32 a = 0;
11l
11m
a = a < in ? in : a;
12m
11n
counter = counter + 1;
12n
counter.valid = in.valid;
11o
return counter == numOfData ? a : INVALID;
12o
}
st (EID_FLOW_0, 0, "output", 4, 1)
= max (EID_FLOW_0, Id(EID_FLOW_0, 0, "input", 0x400, 0x100));
10e

Fig. 11

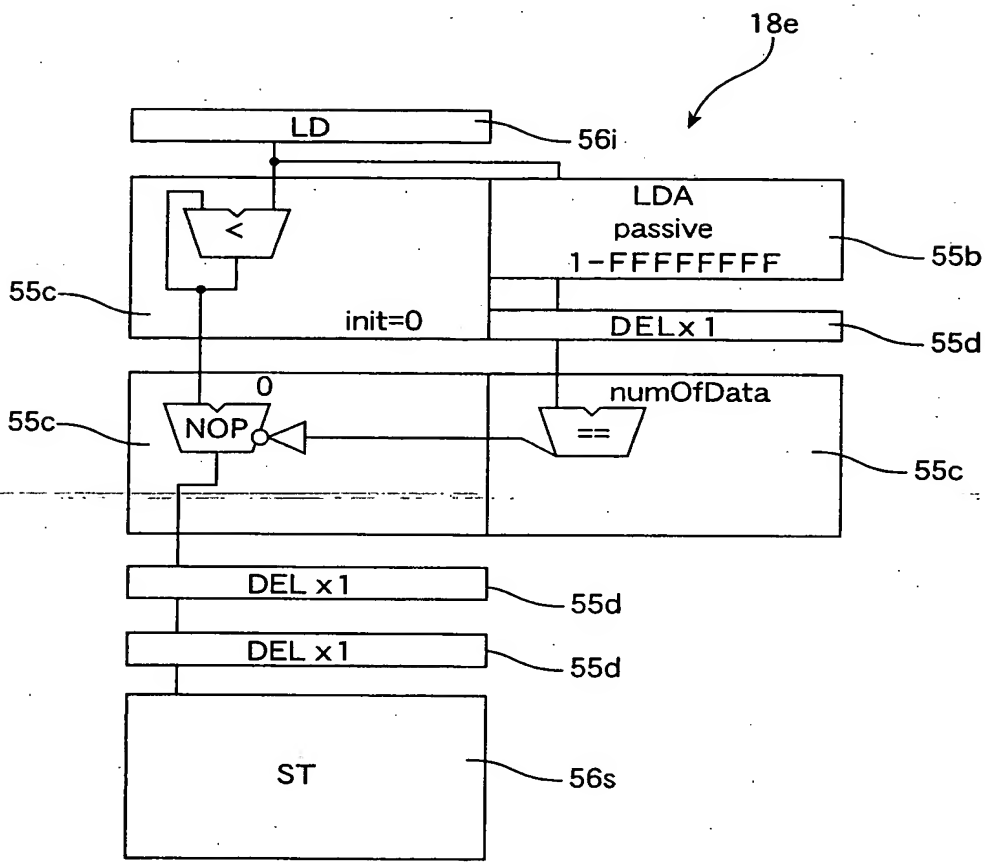

18e
LD
56i
LDA
passive
1-FFFFFFFF
55b
<
55c
init=0
DELx1
55d
0
numOfData
55c
NOP
==
55c
DEL x1
55d
DEL x1
55d
ST
56s

Fig. 12

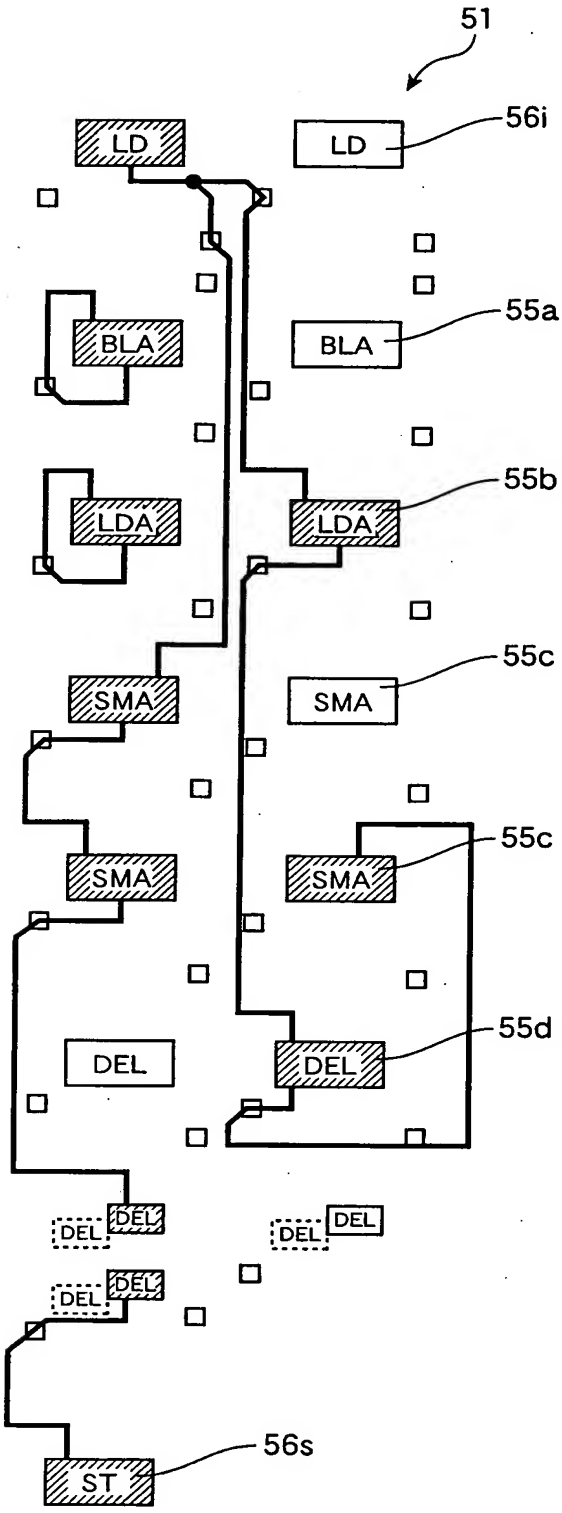

51
LD
LD
56i
BLA
BLA
55a
LDA
LDA
55b
SMA
SMA
55c
SMA
SMA
55c
DEL
DEL
55d
DEL
DEL
DEL
DEL
DEL
DEL
56s
ST

Fig. 13

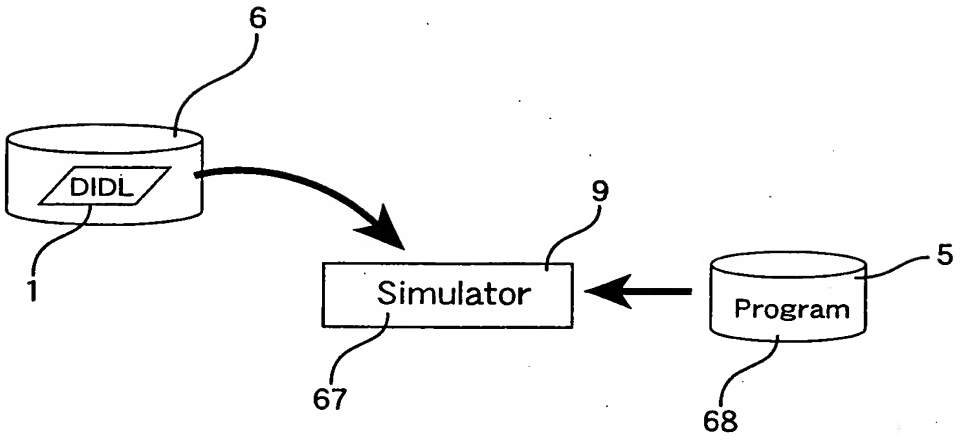
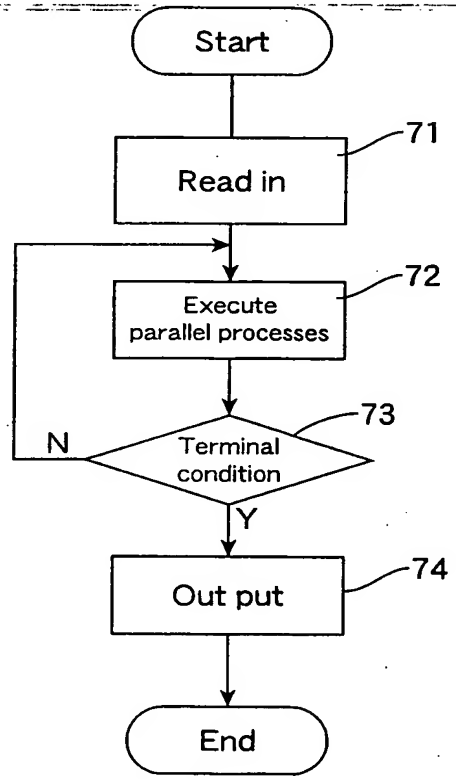

6
DIDL
1
9
Simulator
67
5
Program
68

Fig. 14


Start
71
Read in
72
Execute parallel processes
73
N
Terminal condition
Y
74
Out put
End